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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/996,462

11/28/2001

Desmond R. Lim

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GAUTHIER & CONNORS, LLP

225 FRANKLIN STREET

SUITE 2300

BOSTON, MA 02110

EXAMINER

WONG, TINA MEI SENG

ART UNIT

PAPER NUMBER

2874

MAIL DATE

DELIVERY MODE

07/09/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

09/996,462

**Applicant(s)**

LIM ET AL.

**Examiner**

Tina M. Wong

**Art Unit**

2874

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 December 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 April 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION*****Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08 December 2004 has been entered.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1-6, 9-11, 18-22 and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over an article in Journal of Lightwave Technology, Volume 17 No. 9 titled High-Density Integrated Optics to Manolatos et al.**

In regards to claims 1-6, Manolatos et al. discloses an optical cavity with an input port and an output port that interconnects polySi waveguides with an interconnecting structure that is a five-sided polygon with straight edges that are orthogonal and finite in width. Manolatos et al. additionally discloses the interconnecting structure to reflect the input signals at a 45 degree angle, to interconnect the first and second waveguides at 90 degrees and the fifth side of the polygon structure to be aligned at an angle of 135 degrees from both of its respective sides.

In regards to claims 9-11 and 18-22, Manolatos et al. discloses an optical splitting device as a T-shaped or Y-shaped with an input port which received an input polySi wavelength that is split into at least two signals and directed to at least two output polySi waveguides. The splitting structure also includes at least two separate cavities connected to their sides where each cavity includes five straight edges that are orthogonal, however put together is a seven-sided polygon. Furthermore, Manolatos et al. discloses the seven sided polygon cavity to have two sides that are aligned at angles of 135 degrees and 270 degrees with their respective adjacent sides.

In regards to claims 29-32, Manolatos et al. discloses an optical resonator with a plurality of straight polySi waveguides and a plurality of interconnecting elements, where the interconnecting elements are five-sided polygons that have orthogonal edges and a finite width. Additionally, Manolatos et al. discloses the fifth side of the polygon to be aligned at an angle 135 degrees from both of its respective sides.

But in regards to claims 1, 9 and 29, Manolatos et al. fails to specifically disclose a three-dimensional interconnecting structure with a finite thickness. However, in the introduction of the article in column 2, Manolatos et al. discloses in the article, only two-dimensional geometries are discussed for ease in computation. Furthermore, a three dimensional cavity would have a finite height, finite width and finite thickness. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have altered the two-dimensional cavity to a three dimensional cavity with a finite thickness.

**Claims 7, 12, 14-17, 23, 25-28 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over an article in Journal of Lightwave Technology, Volume 17 No. 9 titled High-Density Integrated Optics to Manolatos et al. as applied to claims 1, 9 and 29 above,**

**and further in view of an article in Optoelectron, Volume 143 No. 5 titled Development of a Library of Low-Loss silicon-on-insulator optoelectronic devices to Tang et al.**

Manolatos et al. discloses all discussed above, but Manolatos et al. fails to disclose the input and output waveguides to be SOI (silicon-on-insulator) waveguides having a silicon core, a cladding of silica and a top cladding layer of air. Manolatos et al. also fails to disclose the polySi waveguides disclosed to have a silicon core, a cladding layer of silica and a top layer cladding of air. However, Tang et al. does disclose SOI waveguide technology to be used in waveguides, couplers, junctions and modulators. SOI is just a different type of waveguide as the polySi disclosed by Manolatos et al. so, therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used either a polySi waveguide or a SOI waveguide in an optical cavity structure, optical resonator or an optical splitter. Additionally, it is disclosed by Tang et al. and also well known in the art that a commonly used waveguide core material is silicon, a commonly used waveguide cladding layer materials are air and silica. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used a waveguide having a silicon core, a cladding of silica and a top cladding layer of air.

**Claims 8, 13, 24 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over an article in Journal of Lightwave Technology, Volume 17 No. 9 titled High-Density Integrated Optics to Manolatos et al. as applied to claims 1, 9 and 29 above, and further in view of U.S. Patent 5,949,931 to Kitamura.**

Manolatos et al. discloses all discussed above, but Manolatos et al. fails to mention an interconnecting structure being etched using anisotropic etching. However, Kitamura discloses

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an optical coupler, also used to interconnect fibers, to be etched by method of anisotropic etching. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have an interconnecting structure being etched using anisotropic etching.

### ***Response to Arguments***

Applicant's arguments filed 08 December 2004 have been fully considered but they are not persuasive.

Applicant argues Manolatu fails to disclose a three-dimensional interconnecting structure with a finite thickness. The Examiner disagrees. In the introduction of the article in column 2, Manolatu et al. discloses in the article, only two-dimensional geometries are discussed for ease in computation. However, this does not limit the geometry to simply a two-dimensional interconnecting structure.

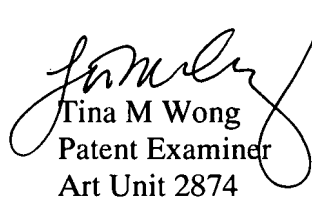
In response to the Examiner's argument that Manolatu et al's structure is not limited to a two-dimensional interconnecting structure, Applicant argues the structure does not include a thickness "because of the inherent limitation that two-dimensional structures do not have a thickness." However, the Examiner disagrees. The Examiner would argue in a three dimensional place, in which the structure would currently reside, every structure, including two-dimensional structures, would have a thickness, even if this thickness is small, thin or negligible. The two-dimensional structure described by Manolatu et al is described in the two-dimensional sense for ease of computation. The Examiner would argue the Manolatu et al structure would inherently have a third dimension/thickness since the structure currently resides in a three dimensional place.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tina M. Wong whose telephone number is (571) 272-2352. The examiner can normally be reached on Monday-Friday 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Tina M Wong  
Patent Examiner  
Art Unit 2874